

ELEG 549: VLSI Testing

Semester: Spring 2012.
Class Time: Mon. Wed. 11:00am-12:15pm.
Classroom: Mandeville Hall, Room 308.
Instructor: Xingguo Xiong (Associate Professor)
Office: Technology Building, Room 140.
Office Hours: Tue. Thur. 3:00pm-4:00pm, Wed. 4:30pm-5:30pm.
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Course Website: UB Blackboard, URL: <http://blackboard.bridgeport.edu/webapps/login/>

Description: As VLSI continues to grow in its complexity, VLSI testing and design-for-testability are becoming more and more important issues. This course will cover VLSI testing techniques such as VLSI fault modeling (stuck-at-fault), logic and fault simulation, automatic test generation, memory testing, delay testing, design for testability (DFT), etc. VLSI scan testing, built-in self-test (BIST) and boundary scan standard will also be covered. Students will learn various VLSI testing strategies and how to design a testable VLSI circuit.

Credit: 3.0.

Textbook: M. L. Bushnell and V. D. Agrawal, *Essentials of Electronic Testing for Digital, Memory, and Mixed-Signal VLSI Circuits*, Kluwer Academic Publishers, 2000, ISBN: 0792379918.

Reference: Laung-Terng Wang, Charles Stroud, and Nur A. Touba, *System-on-Chip Test Architectures (Systems on Silicon)*, Morgan Kaufmann Publishers, Nov. 16, 2007, ISBN: 0123-73973-X, ISBN 13: 978-0123-73973-5.
Laung-Terng Wang, Cheng-Wen Wu, and Xiaoqing Wen, *VLSI Test Principles and Architectures: Design for Testability*, Morgan Kaufmann Publishers, Jul. 07, 2006, ISBN-10: 0123705975, ISBN-13: 978-0123705976.
Miron Abramovici, Melvin A. Breuer, and Arthur D. Friedman, *Digital Systems Testing and Testable Design*, Wiley-IEEE Press, Sept. 1994, ISBN-10: 0780310624, ISBN-13: 978-0780310629.
N. K. Jha, and S. Gupta, *Testing of Digital Systems*, Cambridge University Press, 1st edition, Jun.15, 2002, ISBN-10: 0521773563, ISBN-13: 978-0521773560.
Jan M. Rabaey, *Digital Integrated Circuits: A Design Perspective*, Prentice Hall, 1996, ISBN: 8178089912.
John F. Wakerly, *Digital Design: Principles and Practices*, 4th edition, July 27, 2005, Prentice Hall, ISBN: 0131733494.

Goals: The goal of this course is to help students get familiar with knowledge and skills in VLSI testing and validation. Students will learn VLSI fault modeling, testing strategies for combinational/sequential circuits, memory, and analog circuits. Some important topics such as delay testing, design for testability (DFT), built-in self-test (BIST) and boundary scan standard will also be discussed. Upon completion of this course, students will be able to effectively test VLSI systems using existing test methodologies, tools and equipments.

Prerequisites: Background knowledge in Digital VLSI.

Topics :

1. VLSI Testing Process and Test Equipment.
2. Test Economics and Product Quality.
3. Fault Modeling (single stuck-at-fault, etc).
4. Logic and Fault Simulation.
5. Testability Measurements.
6. Combinational Circuit Test Generation.
7. Sequential Circuit Test Generation.
8. Memory Testing.
9. Delay Testing.
10. IDDQ Testing.
11. Design for Testability.
12. Digital DFT and Scan Design.
13. Built-In Self-Test.
14. Boundary Scan Standard.
15. System Test and Core-Based Design.

Grading: The final grade will be 15% on homework, 15% on projects, 31% on mid-term exam, 35% on final exam, and 4% on attendance. There are four times of random attendance during the whole semester. Each attendance will be counted 1 point toward your final grade.

Exams: There will be two exams: the mid-term exam and the final exam.

Software Usage: VLSI EDA tools (Synopsys tools, Cadence OrCAD PSPICE, etc.) will be used for projects.

Lab Projects: Projects on VLSI testing will be assigned. The goal of the projects is to help student accumulate skills and experience in VLSI testing and validation. Students will use the knowledge they learned in the class for the testing and fault simulation of various VLSI circuits. Synopsys software and other VLSI EDA tools may be used in the course projects.

Cheating Policy: It is the student's responsibility to familiarize himself or herself with and adhere to the standards set forth in the policies on cheating and plagiarism as defined in Chapters 2 and 5 of the Key to UB (<http://www.bridgeport.edu/pages/2623.asp>) or the appropriate graduate program handbook.