ELEG-548: Low Power VLSI Circuit Design

Semester: Fall 2012.
Class Time: Mon. Wed. 11:00am-12:15pm.
Classroom: Mandeville Hall, Room 318
Instructor: Xingguo Xiong (Associate Professor)
Office: Tech 140.
Office Hours: Tue. 3:00pm-4:00pm, Mon. Wed. 4:30pm-5:30pm.
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Course Website: UB Blackboard, URL: http://blackboard.bridgeport.edu/webapps/login/

Description: With the rapid development of mobile computing, low power VLSI design has become a very important issue in the VLSI industry. A variety of low-power design methods are employed to reduce power dissipation of VLSI chips. This course is designed to cover low-power design methodologies at various design levels (from system level to transistor level). The basic low-power design strategies will be introduced in the class. Students will use the learned knowledge to design low-power VLSI circuits.

Credit: 3


Goals: Upon completion of this course, students will be able to analyze the power consumption of VLSI circuits, and design low-power VLSI circuits using various strategies at different design levels. The major target is to design VLSI chips
used for battery-powered systems and high-performance circuits not exceeding power limits.

**Prerequisites:** Fundamentals of microelectronics.

**Topics:**

1. Modeling and sources of power consumption
2. Power estimation at different design levels (circuit, transistor, and gate levels)
3. Power optimization for combinational circuits
4. Power optimization for sequential circuits
5. Power optimization for RT and algorithmic levels
6. Circuit and layout level for low power
7. Software design for low power
8. Low power random access memory circuits
9. Leakage power consumption in deep sub-micron technologies
10. Power analysis and design at system level
11. Case studies
12. Other up-to-date research topics

**Grading:**

The final grade will be 15% on homework, 15% on projects, 31% on mid-term exam, 35% on final exam and 4% on attendance. There will be four random attendance, each will count 1 point in your final grade.

**Exams**

There will be two exams: the mid-term exam and the final exam.

**Computer Usage:** VLSI EDA tools (PSPICE, Synopsys, Mentor Graphics Tools, etc.).

**Lab Project:** Three lab projects on low power VLSI design and simulation will be assigned. The goal of the projects is to help student accumulate skills and experience in low power VLSI design. Students will implement the low power strategies they learned from the class in their circuit design. EDA tools (PSPICE, Synopsys, Mentor Graphics Tools, etc.) will be used for the projects. Software tutorials will be given before the projects. Through these projects, students will know how to estimate the power consumption of a circuit, and how to reduce the power consumption in their design. Example projects include power analysis of CMOS adder, power optimization of FSM, etc. The final project can be the design of a reasonable-size low-power digital system and simulation of its power consumption.

**Cheating Policy:** It is the student’s responsibility to familiarize himself or herself with and adhere to the standards set forth in the policies on cheating and plagiarism as defined in Chapters 2 and 5 of the Key to UB (http://www.bridgeport.edu/pages/2623.asp) or the appropriate graduate program handbook.