Mentor Graphics OPAMP Simulation Tutorial

--Xingguo Xiong

In this tutorial, we will use Mentor Graphics tools to design and simulate the performance of a two-stage OPAMP. The two-stage OPAMP is shown below, which comes from section 5.1 of the book by Johns and Martin.

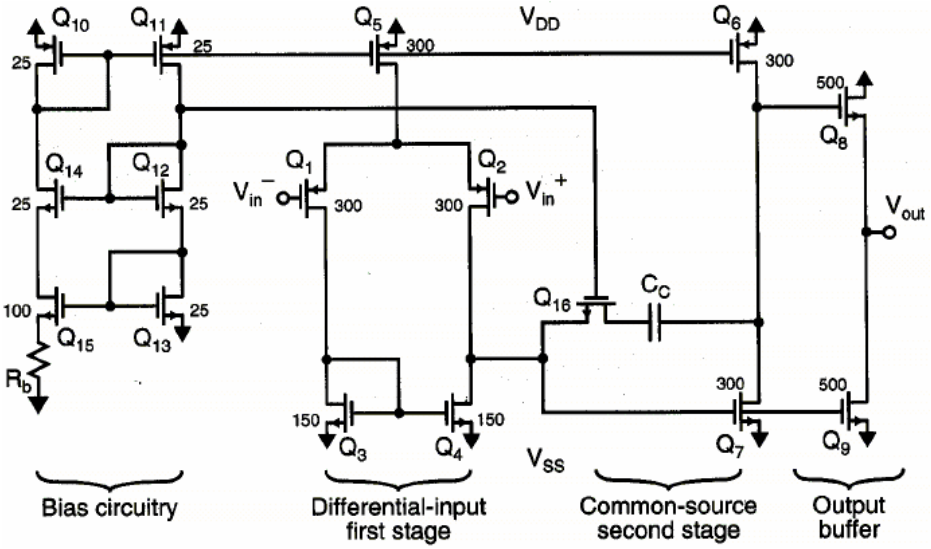


Figure 1. CMOS two-stage amplifier. All transistor lengths are 1.6μm

The procedures for our OPAMP simulation are listed as follow.

1. Use *Design Architecture (DA)* for schematic design.
2. Use *Design Viewpoint Editor (DVE)* for creating design viewpoint for your circuit.
3. Use *Accusim* for OP, Transient, and AC simulation.

Section A. Mentor Graphics Design Architect (DA) for Circuit Design

We are going to use Mentor Graphics Design Architect (DA) tool to design the schematic of the two-stage OPAMP.

1. First we need to decide the sizing (width W and length L) of each transistor in DA schematic design. The sizing of the transistors are listed in unit of micron in Figure 1. However, in DA schematic design, we use unit of lambda (λ). Thus we need to change the sizing of the transistors into lambdas. The lambda value is decided by the technology you use for the fabrication. Here we use AMI C5N technology. The C5N process has a feature size of 0.60 micron, which corresponds to a lambda (λ) value of 0.30μm. Thus we can change the unit of transistor size into lambda by dividing the sizing by 0.30μm. For example, as shown in Figure 1, all the transistors have length of 1.6μm. In this way,
L=1.6μm/0.3μm=5.3λ
Similarly, you can perform such transformation for all the sizing of the transistors. Also please note that if the gates of two transistors are connected together, they will be drawn as shown in Figure 2. So if you see such drawing in Schematic, please be aware that this indicates the gates of two transistors (Q1 and Q2) are connected together. It does not mean that the bulk of transistor Q1 is connected to the gate of Q2.

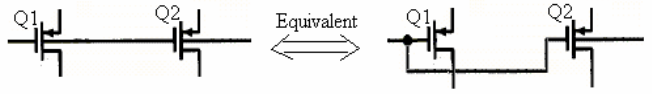


Figure 2. Common gate connection in schematic

Further, in a CMOS analog circuit, the bulk of all PMOS transistors should be connected to the highest voltage level (Vcc), and the bulk of all NMOS transistors should be connected to the lowest voltage level (Vss). Vcc and Vss are the positive and negative power sources of the circuit (here we have Vcc=2.5V, Vss=-2.5V). Considering above information, the schematic of OPAMP in Design Architect is shown in Figure 3.

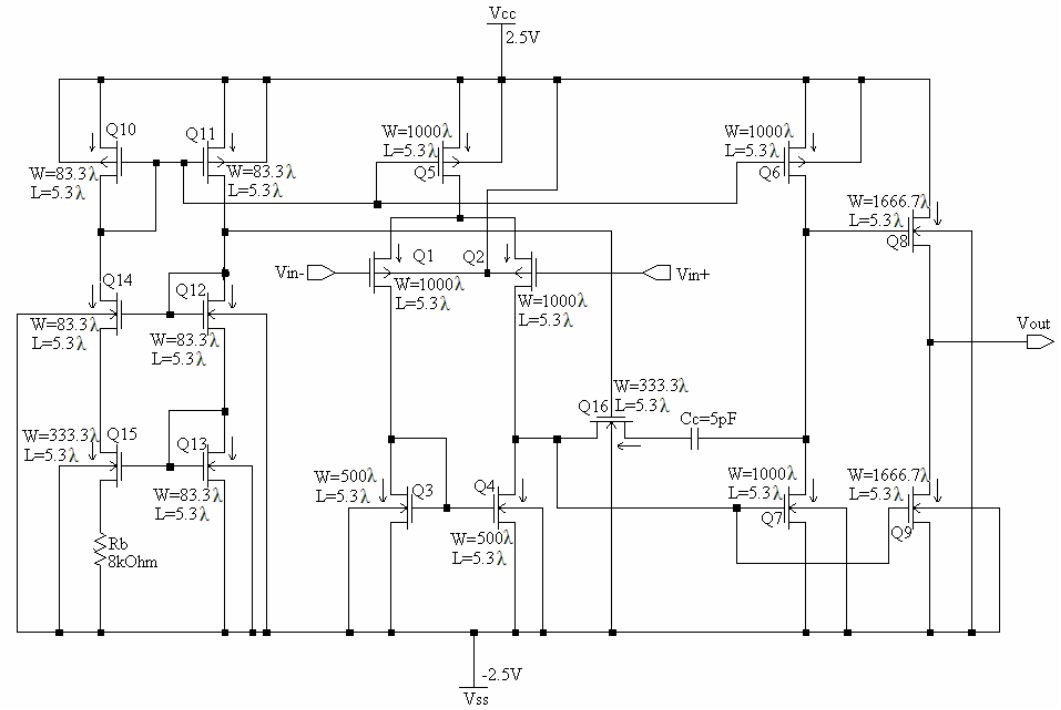
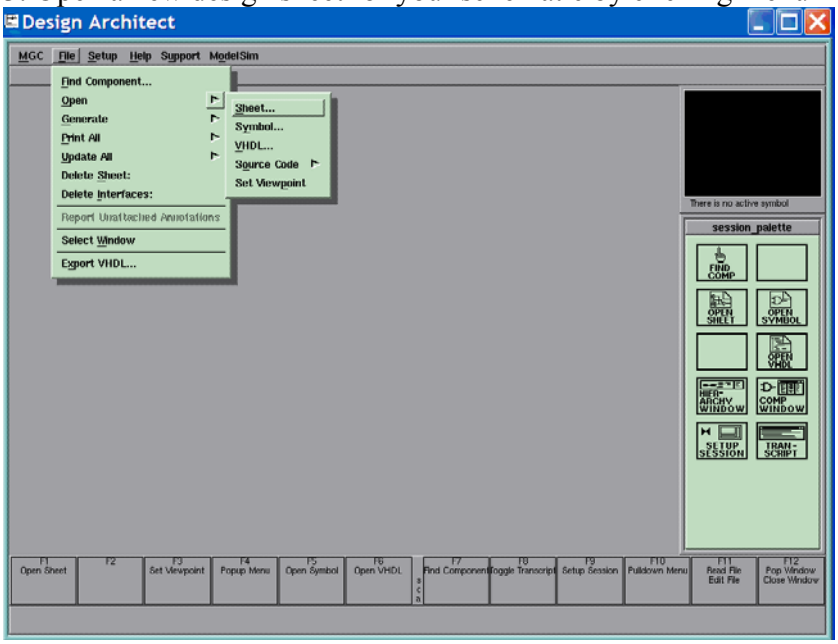
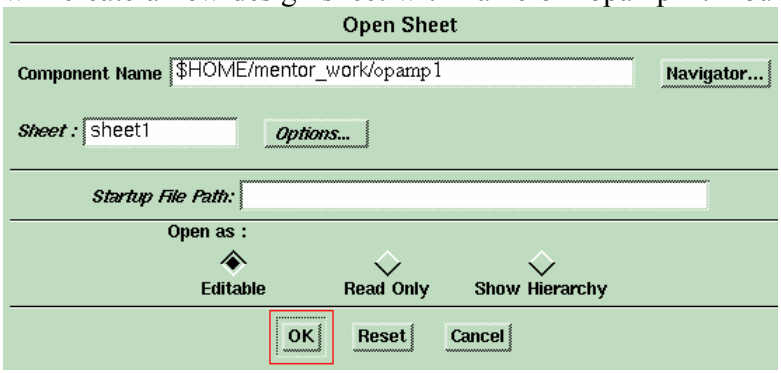


Figure 3. OPAMP design in Design Architect with transistor sizes in unit of lambda

2. Now log into a Unix machine. Open a terminal console window. Input the following command:
da
You will see the main interface of DA tool shows up. Resize the DA window so it will cover most of your screen.
3. Open a new design sheet for your schematic by clicking menu “File—Open--Sheet”.

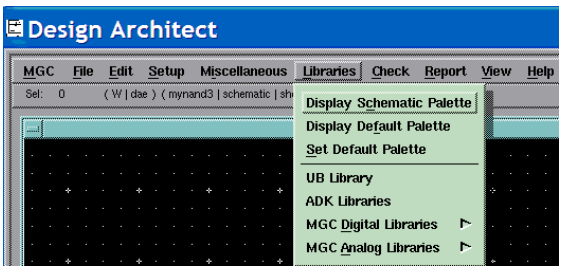


In the popup window, click at the end of the text in the "Component Name" box and type: /opamp1. This will create a new design sheet with name of "opamp1". You can use any name you like for your design.



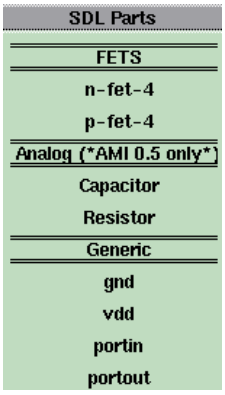
Then click on "OK". You should get a clean schematic sheet. Maximize the sheet window so that you feel comfortable with it.

4. For our circuit schematic design, the procedures are described as follow:
(1). Place all the parts,
(2). Move or rotate/flip some devices if necessary.
(3). Make the wire connections among these parts.
(4). Name/label the nets or input/output ports.
(5). Set part properties (such as resistor and capacitor values, transistor width W and length L, voltage source values of Vcc and Vss, etc.).
(6). Check our design.
All these procedures are described in detail in our previous Mentor Graphics tutorial. Thus we will not cover the details for them. Please refer to our previous tutorial.
First we are going to place all the parts. In this circuit, we need the following parts: six "p-fet-4" (4-terminal PMOS transistors), ten "n-fet-4" (4-terminal NMOS transistor), one resistor, one capacitor, power Vcc and Vss, two input ports "portin", and one output port "portout". Click on menu "Libraries--ADK Libraries".



The ADK_Library palette shows up on the right side:

Click on palette "SDL Parts", you will see the available parts in "SDL library", such as n-fet-4 (4-terminal NMOS), p-fet-4 (4-terminal PMOS, gnd (ground), Vdd (power source), portin (input port), portout (output port), etc.

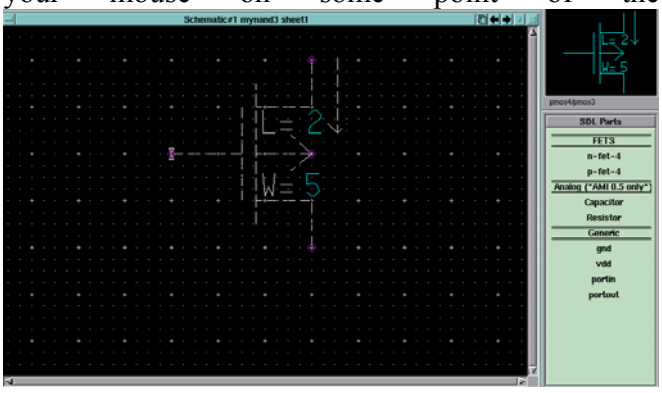


We can use n-fet-4 and p-fet-4 for the NMOS and PMOS transistors in our design, and use portin/portout for input/output port(s). Although here we see the parts of "Capacitor" and "Resistor", we may not use them for our design. This is because if you use them, you will need to add the following two lines in your SPICE parameter to define the capacitor and resistor models for them (if you use your own SPICE parameter):

.MODEL NOTCHEDROW C
.MODEL HR R

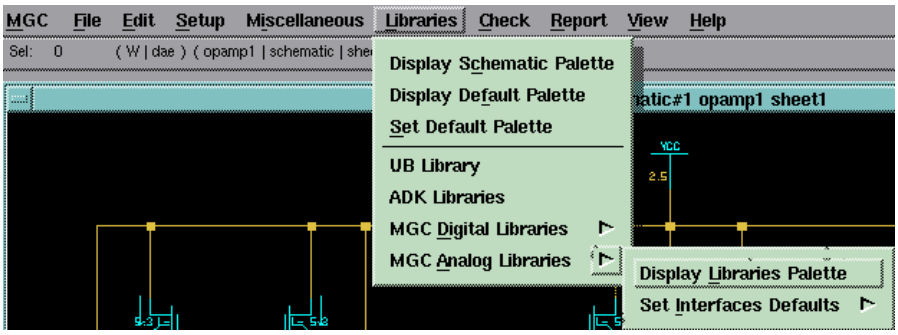
However, if we use the resistor and capacitor from "MGC Analog Libraries—Generic Parts", we needn't define the capacitor and resistor models in our own SPICE parameter file. We will further discuss this later.

5. Please click on the palette "SDL Parts—FETS—p-fet-4", and move your cursor to the design sheet region, you will see a 4-terminal PMOS device shows up and move together with your cursor. Left click your mouse on some point of the sheet to drop it in your design.

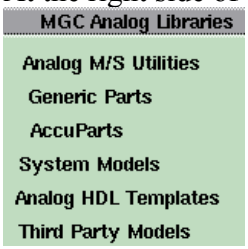


You will see that the PMOS transistor looks too large in your design. This doesn't matter. Just click on menu "View—Zoom out—3.0", you will see the device becomes smaller and you have more space for your design. You may also click on the "maximize" icon (the rectangle in top right corner) to maximize your design view. At this time, you will see the transistor size is defined as "W=5" and "L=2" (the unit is lambda). This doesn't matter. We won't worry about it now because we can adjust it later.

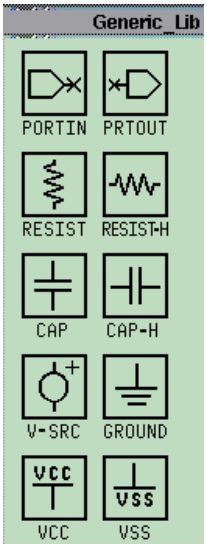
6.Please place all the NMOS/PMOS transistors and portin/portout components from this SDL library. As for power sources Vcc and Vss, resistor and capacitor, please click on menu "Libraries—MGC Analog Libraries—Display Libraries Palette", as shown below.



At the right side of the screen, you will see the palette as below.

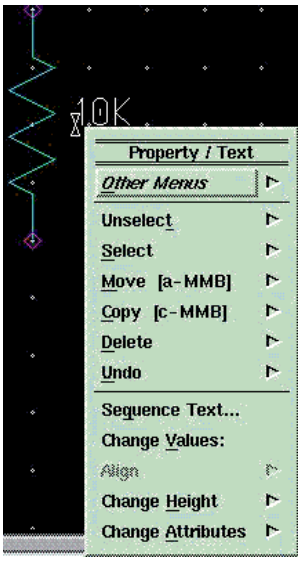


Please click on "Generic Parts", you will see the generic analog parts as below.



Please use the parts of RESIST, CAP, VCC, VSS and GROUND for resistor, capacitor, Vcc, Vss and Ground in our circuit design. If you use the resistor and capacitor parts here, you needn't define the models for them in your own SPICE parameter file. Since we will first perform a DC Operation Point (OP) analysis, we short both input ports (Vin+ and Vin-) to Ground (not Vss). Please insert two "GROUND" parts into your schematic and connect Vin+ and Vin- ports to them. Please note that "Vss" and "Ground" are two different concepts. Vss is the negative power source of the circuit (-2.5V in this example), while "Ground" is analog ground (0V).

7.After you placed all the parts into your schematic, please rotate or flip them as necessary, make the wire connections, and name (label) the input and output ports. Then please set the part properties, such as the sizes (width and length) of transistors, the value of resistors and capacitance, etc. When setting the part properties, please first press "F2" key in your keyboard to unselect all. Then put your mouse pointing exactly on the property value you want to change, and press "F1" key on your keyboard to select it. You will see that the value you want to set changes its color to white, and marked with white double triangles. It's important that you point your mouse exactly on the value you want to change, otherwise you may select the whole device instead of its specific value. Now please right click your mouse. In the popup window, please click to select "Change Values", as shown below. You would get the corresponding popup window so that you change change the value for this property.

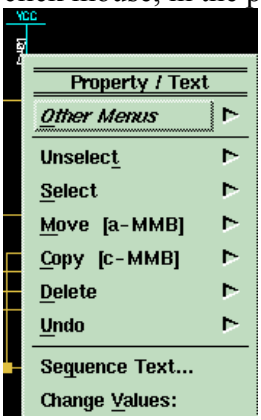


For example, if you point your mouse exactly on the value of "10K" and press "F1" key, you would be able to select it and its color changes into white. Then right click your mouse, in the popup window select "Change Values", you will see the following popup window in the bottom:

In the "New Value" line, change the value of "10K" into "8K", and click OK. You will see the resistor value is changed from 10K to 8K. Similarly, you can also set the capacitor value to the desired value.

8.Now let's change the Vcc and Vss values to 2.5V and -2.5V separately. First press "F2" key in keyboard to unselect all. Take Vcc as an example.

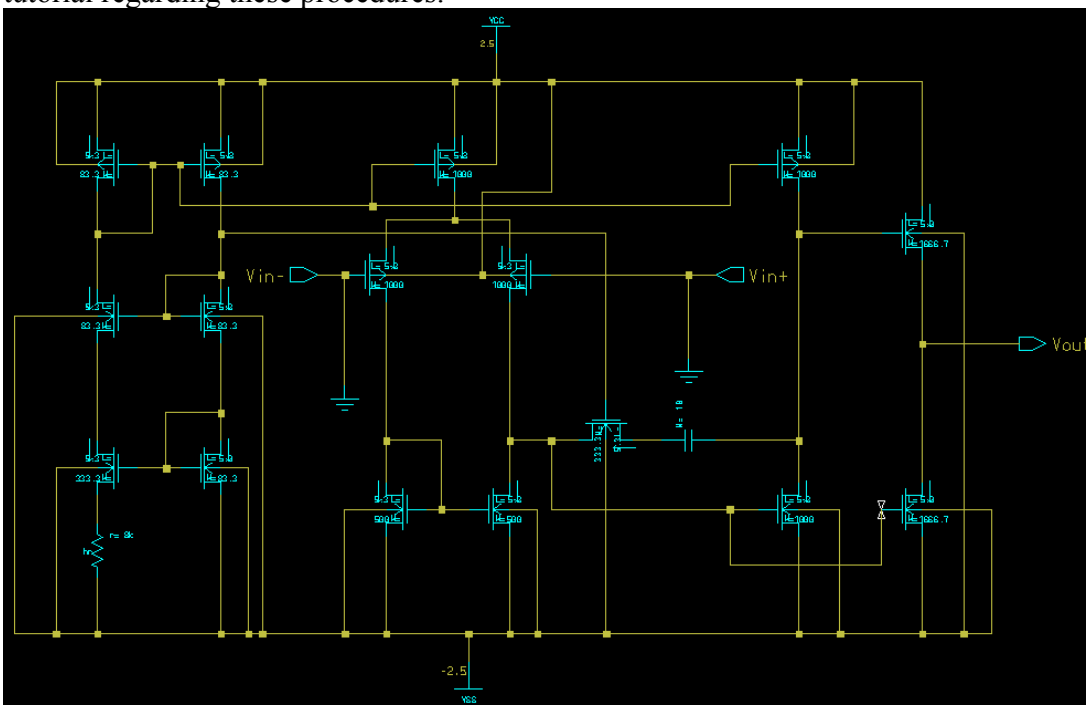
9.Please move your mouse to point exactly on the value "5" of Vcc and click "F1" key in your keyboard to select the value ("5"). You will see white star symbol appearing to show that it is selected. Then right click mouse, in the popup menu, please select "Change Values", as shown below.



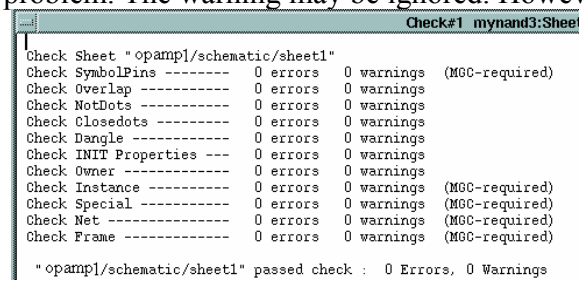
In the new popup window, please type "2.5" as the new value in the "New Value" row, then click OK to close the menu.

You will see that the Vcc value has been changed from 5V to 2.5V. Repeat the similar procedure to change the value of Vss to -2.5V.

10.After you finish all the above procedures, your design should look like follow. All the above procedures are introduced in our previous Mentor Graphics tutorial in detail. Please refer to our previous tutorial regarding these procedures.



11.Now we finished our schematic design. Let's run a check to see whether there is any error in it. Please click menu "Check—Sheet". You will get a check report as follow. Please check the report to see if there is any error. If there is any error, please find out the reason and go back to revise your design to solve the problem. The warning may be ignored. However, you must ensure there is zero error in it.


Check#1 mynand3:Shee

```
Check Sheet "opamp1/schematic/sheet1"
Check SymbolPins --------   0 errors   0 warnings  (MGC-required)
Check Overlap -----------   0 errors   0 warnings
Check NotDots -----------   0 errors   0 warnings
Check Closedots ---------   0 errors   0 warnings
Check Dangle ------------   0 errors   0 warnings
Check INIT Properties ---   0 errors   0 warnings
Check Owner -------------   0 errors   0 warnings
Check Instance ----------   0 errors   0 warnings  (MGC-required)
Check Special -----------   0 errors   0 warnings  (MGC-required)
Check Net ---------------   0 errors   0 warnings  (MGC-required)
Check Frame -------------   0 errors   0 warnings  (MGC-required)

 "opamp1/schematic/sheet1" passed check :  0 Errors, 0 Warnings
```

12. Now click on the top left icon of the report window and select "Close" to close the report window. Click on menu "File—Save sheet" to save your schematic design, and then click on menu "MGC—Exit" to exit Design Architect.

Section B. Creating an ICGraph viewpoint

Now we will create the view point file for Accusim simulation.

13. After you exit "Design Architect", now you come back to "terminal console" command prompt window. First make sure you are in the same directory as your schematic design file. Your schematic design files should be kept in the directory of "/home/your_user_name/mentor_work". You must be in the same directory in order to use the "adk_dve" command to create the ICGraph viewpoint. Please type:

pwd

in terminal console prompt window and enter it. This command will display your current directory. If it's already in your "/home/your_user_name/mentor_work", then you needn't do anything and directly go to next step to create the viewpoint. However, in this example, I found that my current directory is my home directory "/home/xxiong".

```
india% pwd
/home/xxiong
india% 
```

In this way, I type the "ls" command to see the current files and subdirectories in this directory. Please type "ls", and I see the following file/subdirectory display:

```
india% ls
1.txt              album1.html        mgc
AdobeFnt.lst       fft.Svdm_svdb.attr  xfig.SAVE
adk_dve.log        mentor_work        xv1
```

The "mentor_work" directory is there. Then use "cd" command to enter that directory. I enter the command of "cd mentor_work" as shown below:

```
india% cd mentor_work
```

Now I enter command "pwd" again to check my current directory, and find that I am already in the "/home/xxiong/mentor_work" directory.

```
india% pwd
/home/xxiong/mentor_work
india% 
```

14. Now in the prompt window, input the following line:

adk_dve opamp1 –technology ami05

You will see a lot of text scrolling on the screen. Your viewpoint file for your design will be created. The format of "adk_dve" command is:

adk_dve *your_design_name* –technology technology_name

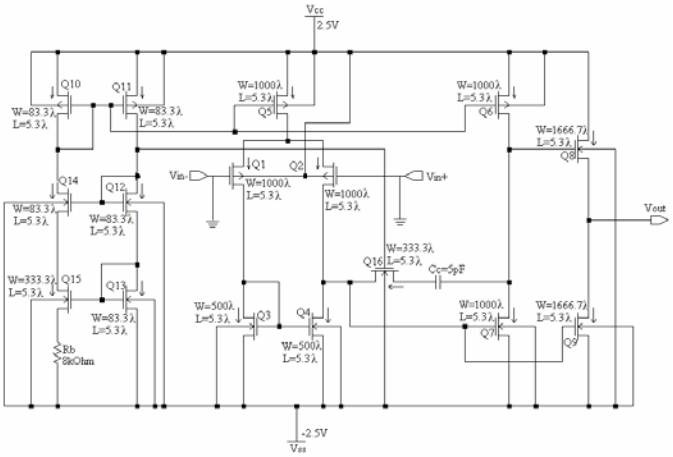
This will create the viewpoint for your design with the technology you want. Here we are using "ami05" technology, which means C5N process with a feature size of 0.6um. The lambda equals half of the feature size, which is 0.3μm.

Section C. ACCUSIM Simulation

Now we are going to use Accusim to simulate our OPAMP schematic. Before you start the Accusim simulation, make sure you have previously created viewpoint file using adk_dve command as described in section B. You need the viewpoint file in order to load the technology parameter (λ) for the correct sizing of the transistors in Accusim simulation. If you make some changes in your design in DA (Design Architect), you need to rerun the *adk_dve* command to create a new viewpoint file. Otherwise, your change in DA may not be reflected in your Accusim simulation. We will perform three analysis: OP operation point analysis, transient analysis, and AC analysis (for Bode plot). The general simulation procedure is: First define the model library, then setup analysis, define forces (input voltages on input ports), and define the keeps (signals to be saved during simulation for observation). Then we click on "Run" to run the analysis. Once the simulation is finished, we select the nodes or device terminals for voltages or current signals we want to observe, and click on "Traces" to trace the voltage or current signals. For DC OP analysis, we can select the node or device terminals we are interested in, and click "Flag monitor" in palette to display the DC biasing voltages/currents.

Part 1. OP Operation Point Analysis

OP Operation Point analysis can give use the DC biasing voltage and current for all the nodes and devices. The circuit connection we use for DC OP analysis is shown below. Both input ports (Vin+ and Vin-) are connected to Ground (not Vss).



1. In terminal console prompt window, input following command:

accusim opamp1/accusim

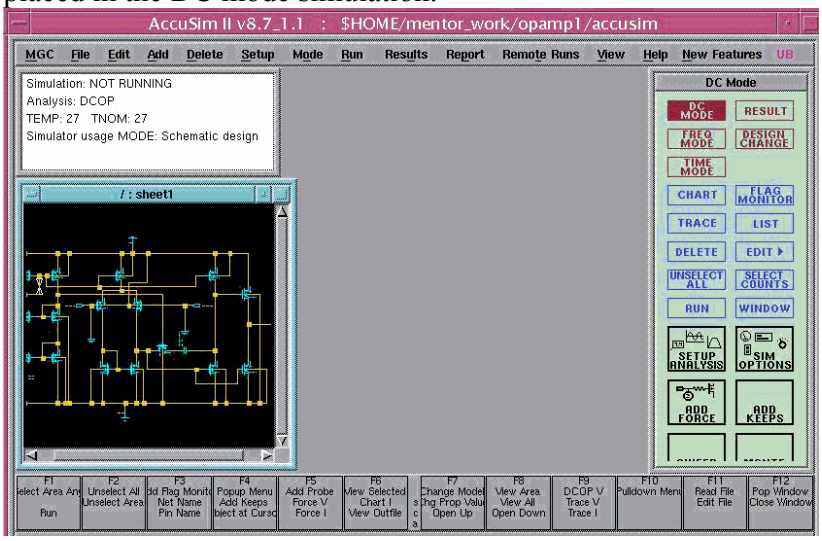
The general command syntax is:
accusim *your_schematic_design_name*/accusim

Please make sure you are not omitting "/accusim" part after your design name. If you omit the "/accusim" part and type the accusim command as follow:

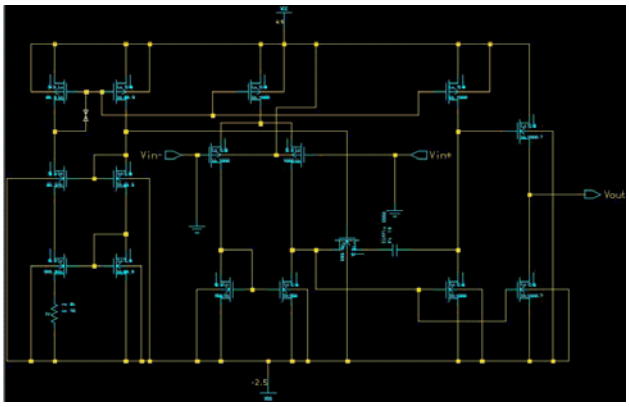
accusim *your_schematic_design_name*

the viewpoint file created by adk_dve command will not be loaded in Accusim. In this way, you will not get correct sizing of the transistors in your netlist, and your simulation result will be wrong.

You should see your schematic design is loaded in a window inside the simulator workspace. You are now placed in the DC mode simulation.



2. In order for DC OP operation point analysis, we connect both input ports (Vin- and Vin+) to ground (not Vss). We already did this in Design Architect, as shown below.



3. Now we need to load a model library to tell Accusim what model should be used for devices such as PMOS/NMOS transistors. We will load our own SPICE parameters for Accusim simulation. Please open a text editor and input following parameters into the file.

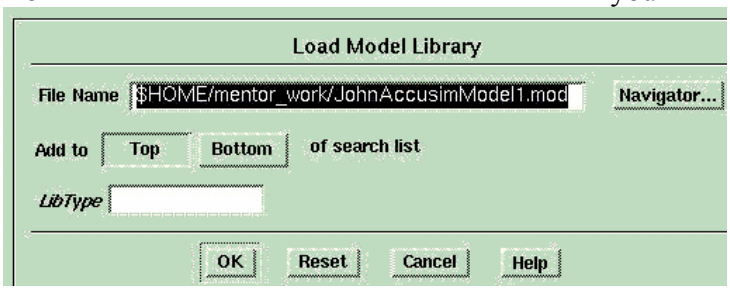
```
**********************************************************************
* SPICE MOSFET Models used in Analog Integrated Circuit Design, by Johns &
* Martin
**********************************************************************
.MODEL n NMOS   LEVEL=3,        TOX=1.8E-8,       LD=0.08U,
+                  UO=500,          VMAX=2.0E5,       PHI=0.6,
+                  GAMMA=0.5,       NSUB=2.5E16,      VTO=0.7,
+                  NFS=8.2E11,      CGSO=2.5E-10,     CGBO=2.5E-10,
+                  CJSW=2.5E-10,    CGDO=2.5E-10,     MJ=0.5,
+                  CJ=2.5E-4,       PB=0.9,           IS=1.0E-16,
+                  JS=1.0E-4        KF=600E-27        AF=0.8
+                  NLEV=2           RS=600            RD=600
+                  ETA=0.05         KAPPA=0.007       THETA=0.06
+                                   XJ=2.7E-7         DELTA=0.7

.MODEL p PMOS   LEVEL=3,        TOX=1.8E-8,       LD=0.08U,
+                  UO=165,          VMAX=2.7E5,       PHI=0.80,
+                  GAMMA=0.75,      NSUB=5.5E16,      VTO=-0.7,
+                  NFS=7.6E11,      CGSO=2.5E-10,     CGBO=2.75E-10,
+                  CJSW=3.4E-10,    CGDO=2.5E-10,     MJ=0.5,
+                  CJ=3.7E-4,       PB=0.8,           IS=1.0E-16,
+                  JS=1.0E-4        KF=400E-27        AF=1.0
+                  NLEV=2           RS=1200           RD=1200
+                  ETA=0.12         KAPPA=1.5         THETA=0.135
+                                   XJ=2.3E-7         DELTA=0.3
```

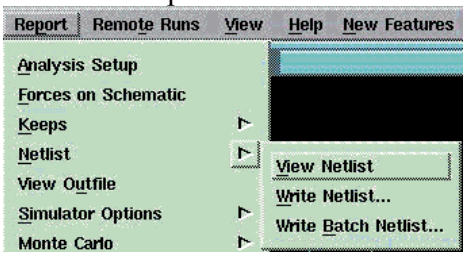
Please save it as “JohnAccusimModel1.mod” to your “$home\mentor_work” directory (You may also use any other name for the model file as you wish). Or you can directly save the “JohnAccusimModel1.mod” file I send to you in your “$home\mentor_work” directory.

4. Now we will load the model file we have created. Click on menu “Files—Auxiliary Files—Load Model Library”, in the dialog box, click “Navigator” to find the “JohnAccusimModel1.mod” in the “$HOME/mentor_work” directory. Click to select it, and then hit “OK”, your “JohnAccusimModel1.mod” will be loaded for use. If you use other name for the model file, please load the corresponding model file

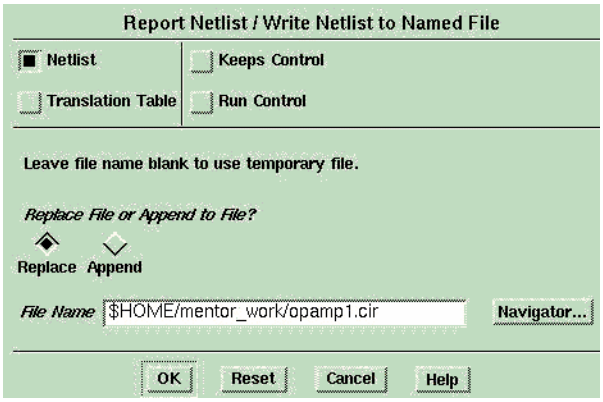
from your directory.



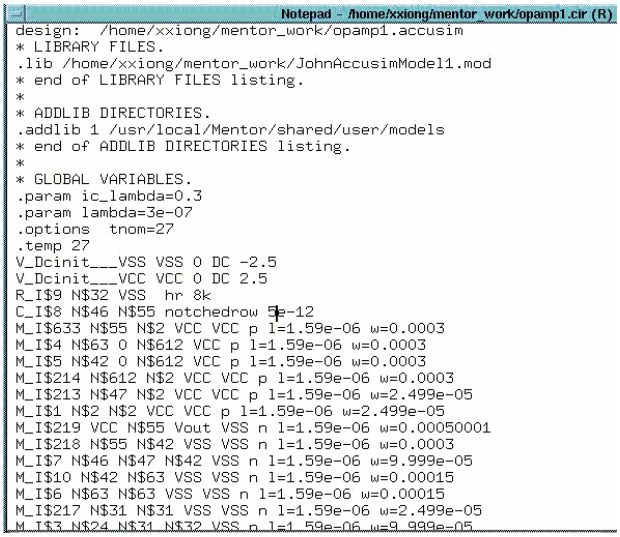
5. Now please check on your SPICE netlist file. Click menu “Report—Netlist—View Netlist”, you can view the netlist file for the OPAMP circuit. If you want to export your SPICE netlist as a file, please click on menu “Report—Netlist—Write Netlist”.



In the popup window, please check “Netlist” and uncheck “Keeps Control”, “Translation Table”, and “Run Control”. In File Name row, please input “$HOME/mentor_work/opamp1.cir”. You can use any other name you like for it. Then click OK.



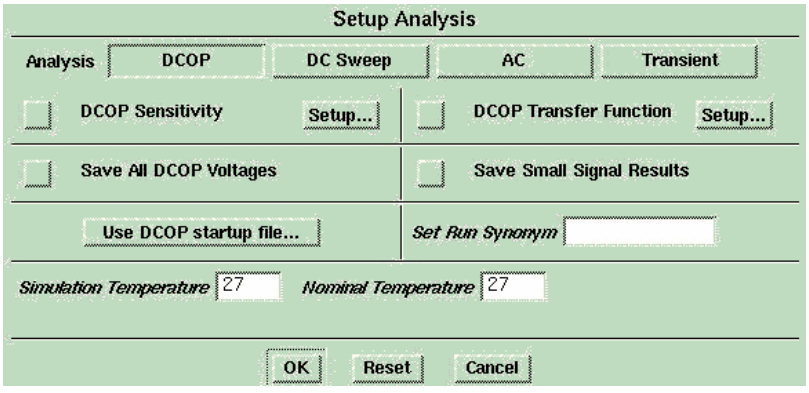
This will generate the SPICE netlist file as “opamp1.cir” in directory “$HOME/mentor_work/opamp1.cir”. You can go to File Manager to open it. It should look like follow.



This SPICE netlist contains all the components and connection information about your circuit. It is helpful for you to debug your design. Please note that since we define the transistor length as L=5.3λ, and we use AMI05 technology with λ=0.3μm, we see the transistor length in SPICE netlist as
$L=5.3\times0.3\times10^{-6}m=1.59E\text{-}6m$
This is very close to our design of L=1.6μm. This slight difference may incur some simulation error, but it's very small. Now please close the netlist file by click on the top left corner of the netlist file and select menu "Close".

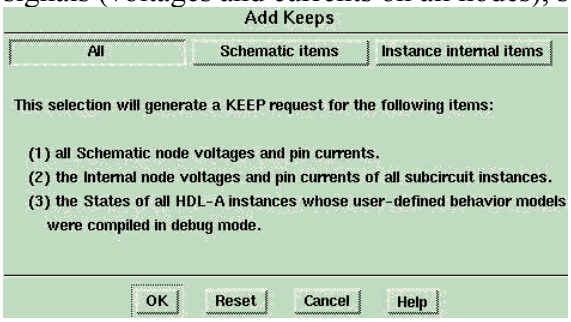
6. Click on the palette "DC Mode", and click on palette "Setup Analysis".

You will see following popup window. Click to select "DCOP" (for DC Operation Point analysis), and click OK to close the window.



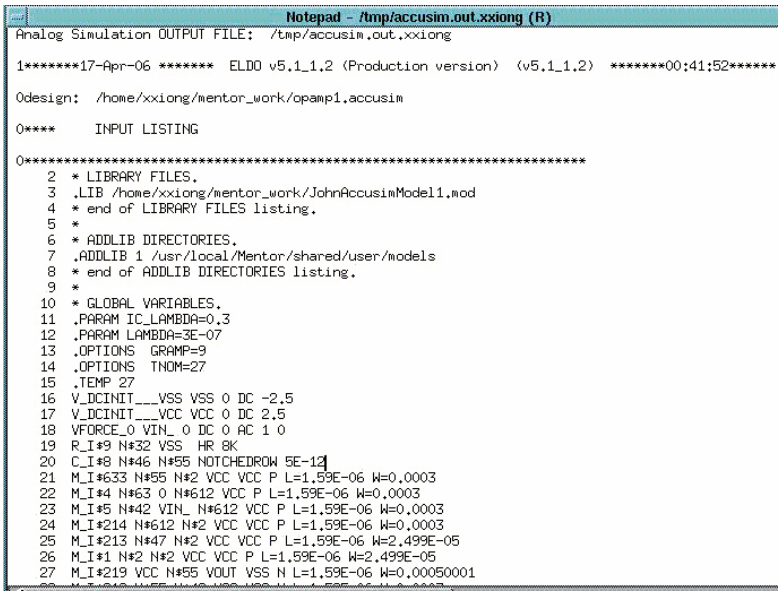
7. Now we will add forces on input ports. Since we are going to perform DCOP (Operation Point) analysis, both input ports (Vin+ and Vin-) are already connected to GROUND in Design Architecture. In this way, we needn't add any forces. Thus we just skip this step.

8. Now we will add keeps to tell Accusim to save the data for the signals we are interested in, so that we can observe their waveforms later. For very large circuit, it may take you tremendous hard drive space to store the data for all the signals. Thus you may only wish to add keeps for some certain signals you are interested in. However, we have a very small circuit in this example. Thus we can choose to add keeps for all the signals. Please click on right palette "Add keeps". You will see following popup window. Please click to select "All", and click OK to close the window. In this way, Accusim will save the data for all the signals (voltages and currents on all nodes), so that we can analyze them later.

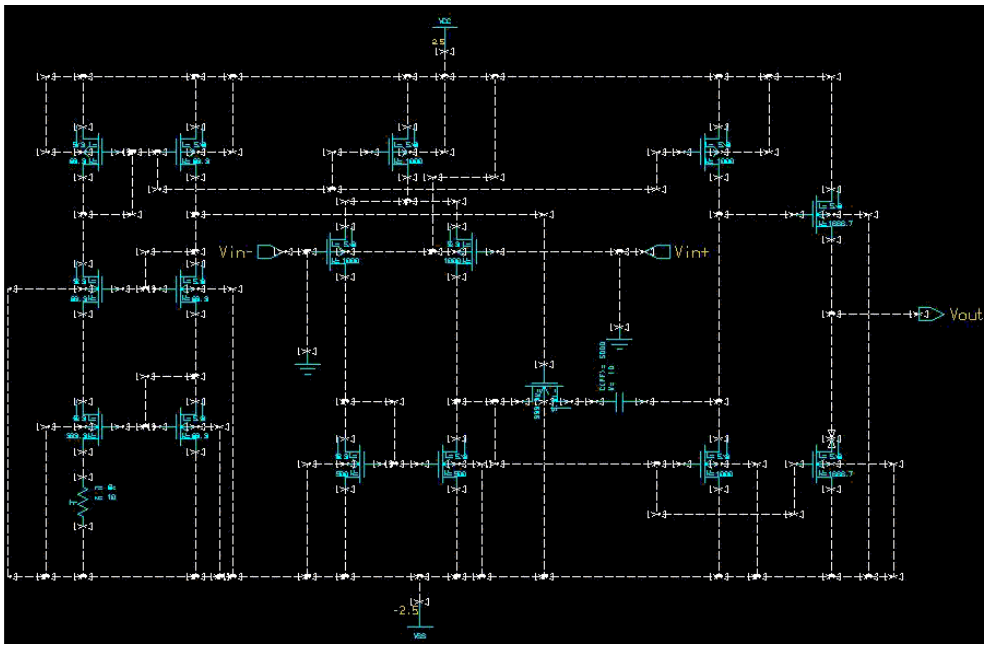


9. Now we are ready for DCOP simulation. Please click on right palette "Run". You will see the mouse cursor changes its shape to indicate that the program is running the simulation. When the simulation is finished, your mouse cursor will recover its normal shape. If there is any error in the simulation, you can click on menu "Report—View Outfile" to see the output file.

You will see the output file as follow. It contains all the information about circuit netlist, possible errors, and simulation results. You can check to see whether it contains any error information. If yes, the error information in it can be very helpful for you to debug the error.

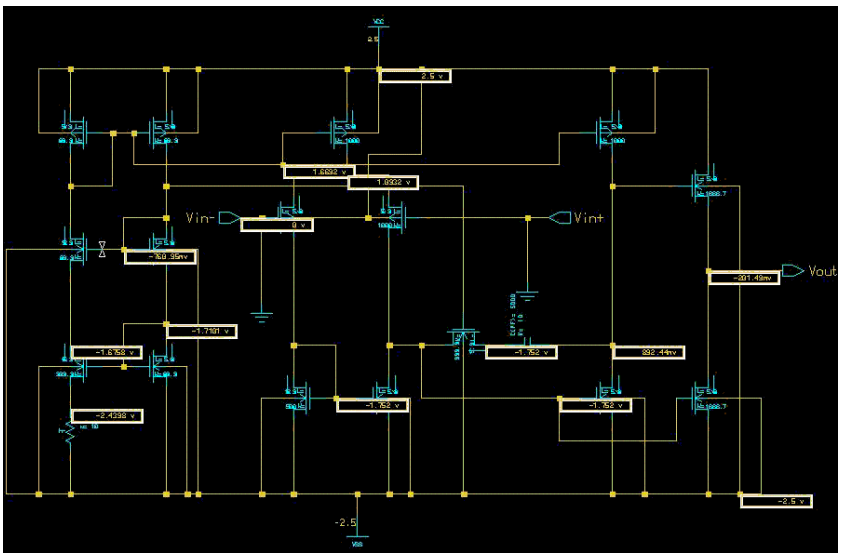


10. Click the top left corner and select menu “Close” to exit the output file window. Now we are ready to observe the DC operation voltages and currents for each node. First we will observe DC voltage biasing for all the nodes. Please left click your mouse on each node to select them, as shown below.

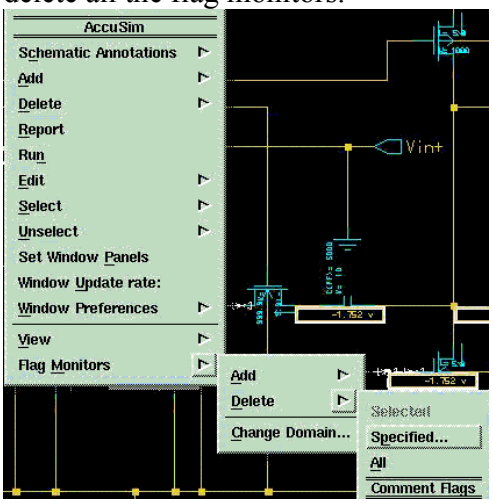


11.Please click on right palette “FLAG MONITOR”, as shown below.

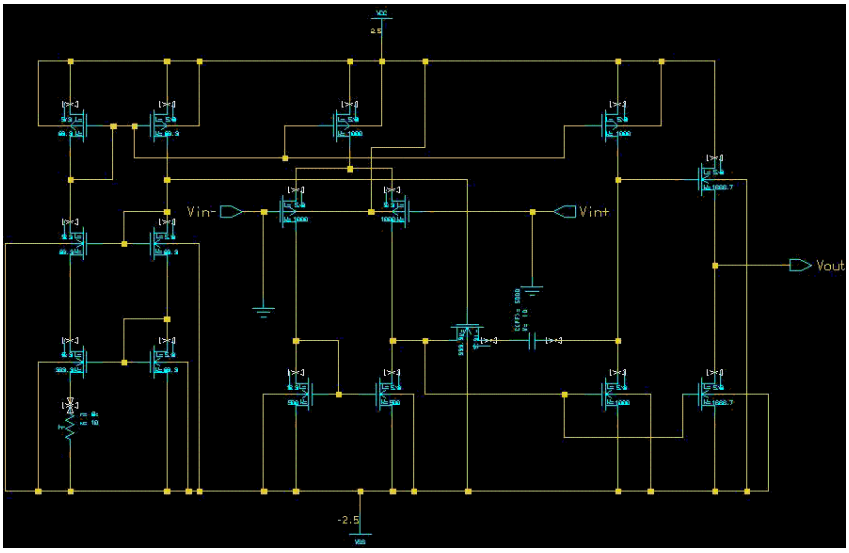
The DC voltage biasing for each node will be listed in white squares, as shown below. Please print out this screen shot. Please note that the DC voltage of output node (Vout) is -201.49mV. If you use your own transistor sizing, or other SPICE parameters, you may get a different value from this result. With the DC biasing voltage on each node, please list a table to calculate the Vgs (for NMOS) or Vsg(for PMOS). With the threshold voltage information from SPICE parameter, please decide the operation mode (triode, active or cutoff) of each transistor. Please make a table to list the operation modes for all the transistors. Except transistor Q16, all other transistors should work in active mode.



12. Now we will delete all the flag monitors and observe the currents through each device. Right click your mouse on anywhere of the circuit, in the popup menu, please select “Flag Monitors—Delete—All” to delete all the flag monitors.

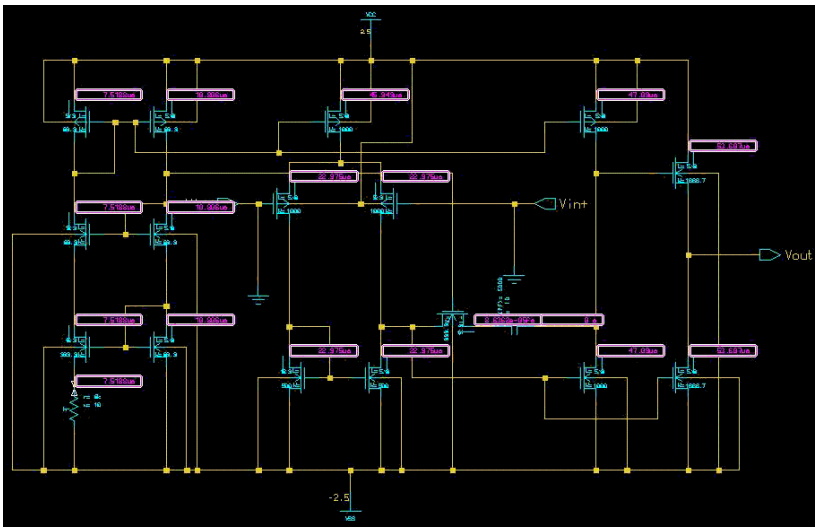


13. We wish to observe the drain or source current through each transistor, and the current through the resistor and capacitor. Please click on the drain or source point of each transistor to select its drain or source terminal (please click exactly on the drain or source point, otherwise you will select the whole node or device instead of its terminal). The selected drain or source terminals of transistors will be marked with double white triangles. Also please click on one end of the resistor and capacitor (you also need to exactly click on the one end of the resistor and capacitor). Your design should look like below with selected device terminals marked with white double triangles.

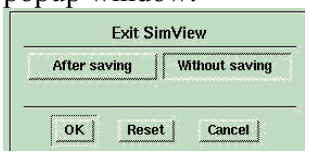


14.Please click on right palette “FLAG MONITOR”, as shown below.

You will see the currents through each selected device terminal is displayed in a white rectangle, as shown below.



15. Please print out the screen shot. After that, right click your mouse on anywhere of the circuit, in the popup menu, please select “Flag Monitors—Delete—All” to delete all the flag monitors.
16. Now we have finished the OP Operation Point analysis. In the next part, we are going to perform the Transient analysis. In transient analysis, we need to break the connection between Vin+ and Ground, and apply Sine wave voltage to input port Vin+. Please note that if you want to make some change to the original circuit, you must do it in Design Architecture. You cannot make change to the circuit schematic in Accusim. Thus we will first exit Accusim, and make changes on the circuit schematic in Design Architect, then come back to Accusim for simulation. Please click on menu “MGC—Exit”, you will see following popup window.



Please click “Without saving”, and click OK to exit Accusim.

Note: Sometimes you get some good simulation result in Accusim and exit the program. Later on you rerun Accusim and simulate the same circuit design again with everything unchanged. However, you may find that are not able to get the result as before. If this is the way, please click Accusim menu “Report—Netlist—View Netlist” to view the netlist file. In the netlist file, please double check whether the transistor sizing is extracted correctly. For example, when you input transistor length as 5.3, you expect to see the transistor length in Accusim netlist as L=1.59e-6. However, if you see L=5.3e-6 in Accusim netlist, this means your netlist is not correctly extracted. This may be the reason that you cannot get the correct waveform for the same design. If this is the case, please exit Accusim. Then in terminal console prompt window, rerun the command:

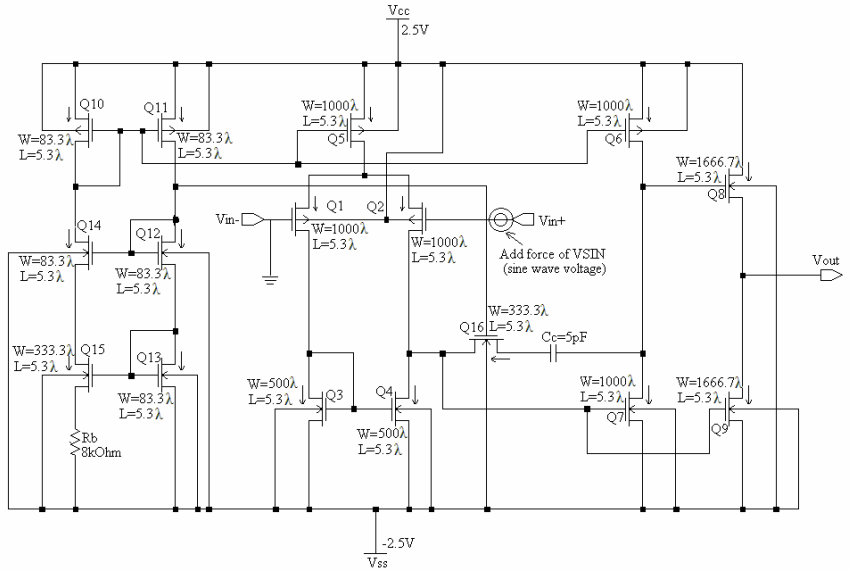
adk_dve your_design_name -technology ami05

Then rerun accusim, double check the netlist file to see whether the transistor sizing is extracted correctly. If it is correctly extracted, then you should be able to get the correct waveform result. Please note that netlist file can always be a very helpful way to debug your design.

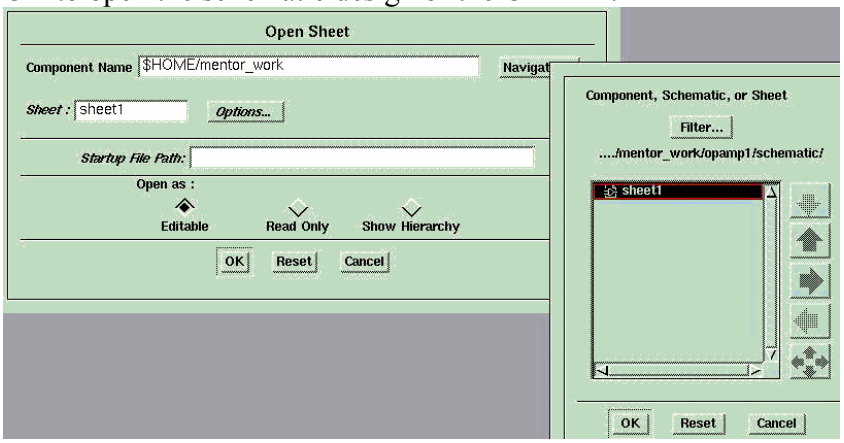
Part 2. Accusim for Transient Analysis

In transient analysis, we are going to find the transient response of the circuit to a small sine wave input voltage on Vin+ port. The magnitude of the sine wave is 10μV, the frequency of the sine wave is 100Hz.

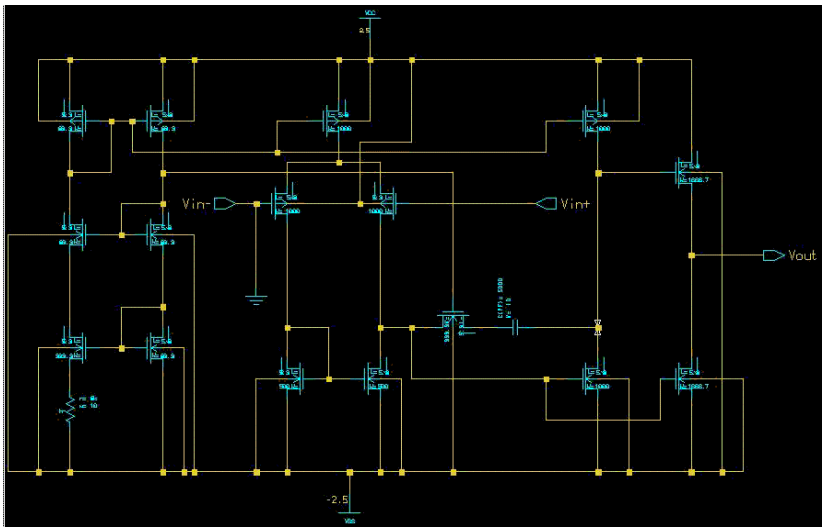
As seen in our following AC analysis, the -3dB frequency of this OPAMP is around several kHz. By selecting the frequency of input sine wave as 100Hz, it is ensured that it will fall into midband region. After transient analysis, by comparing the input/output voltage amplitudes, we can derive the gain of the circuit. By inserting another load resistance between output node (Vout) and Ground and find out the corresponding gain, we can calculate the output resistance R_0 of the OPAMP. The circuit connection for transient analysis (without load resistor) is shown below.



1. In terminal console prompt window, type “da” and press “enter” key to open the interface of Design Architect. In DA main interface, click menu “File—Open--sheet”. In the popup window, click “Navigator”, locate the “$HOME/mentor_work/opamp1” folder (a folder has a letter “c” in its left side), double click it. Again, double click on the “schematic” folder, then double click on “sheet1” file. Click OK to open the schematic design of the OPAMP.

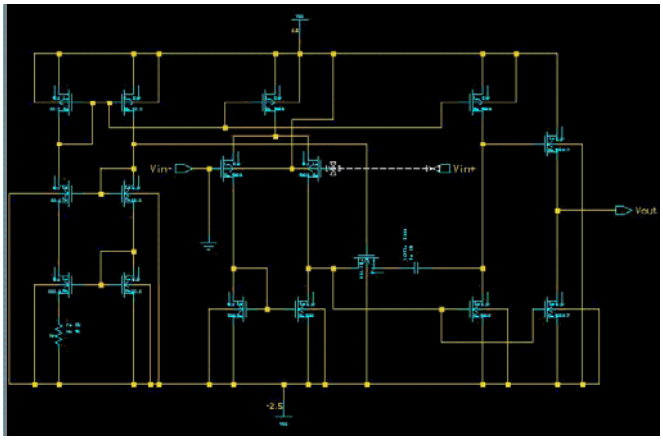


2. In the schematic design, please click to select the GROUND and the corresponding wire connection between Ground and “Vin+” port. Press “Delete” key in keyboard to delete them. Now your schematic should look like below.



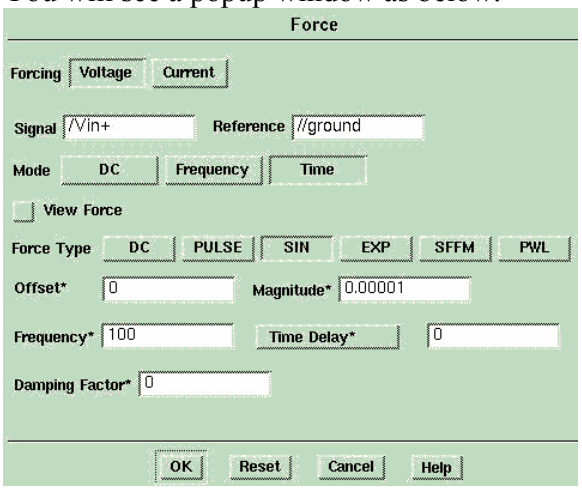
3.Please click menu “File—Save sheet” to save the schematic change.
4.Click menu “MGC—Exit” to exit Design Architect.
5.In the Terminal Console prompt window, type “Accusim opamp1/accusim” to enter the main interface of Accusim. You should see your OPAMP schematic design is already loaded in a window inside the simulator workspace.

6.We are going to load the library model file for Accusim. Click on menu “Files—Auxiliary Files—Load Model Library”, in the dialog box, click “Navigator” to find the “JohnAccusimModel1.mod” in the “$HOME/mentor_work” directory. Click to select it, and then hit “OK”,
7.Now we will add the force (a sine wave input voltage) to Vin+ input port. Please click the wire connected to the input port Vin+ to select the node. The selected node will change into white dotted line, as shown below.



Please click on right palette “Add Force”, as shown below.

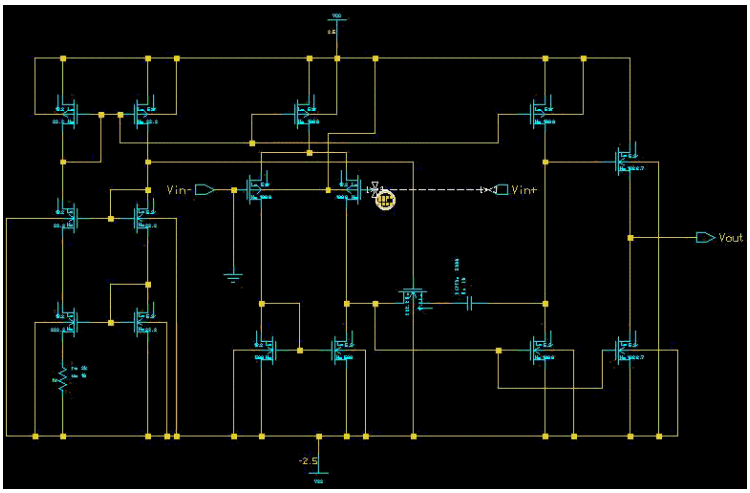
You will see a popup window as below.



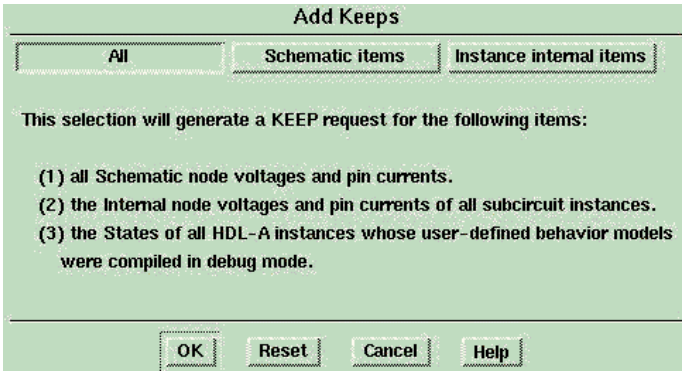
Please note that “voltage” is selected, and the signal is already “/Vin+”, and the reference is “//ground” (this is exactly the reference voltage we use for input voltage on Vin+). Click “Time” in “Mode” line, and click “SIN” in “Force Type” line for sine wave. Type the following input:

Offset: 0
Magnitude: 0.00001
Frequency: 100
Time Delay: 0
Damping Factor: 0

This set the offset voltage as 0V, the magnitude as 0.00001V (10μV), and frequency as 100Hz for the input sine wave voltage on port Vin+. Click OK to close the window. You will see a while circle is added to the node connected to Vin+ port to indicate a force (input stimulus voltage) is applied it, as shown below.



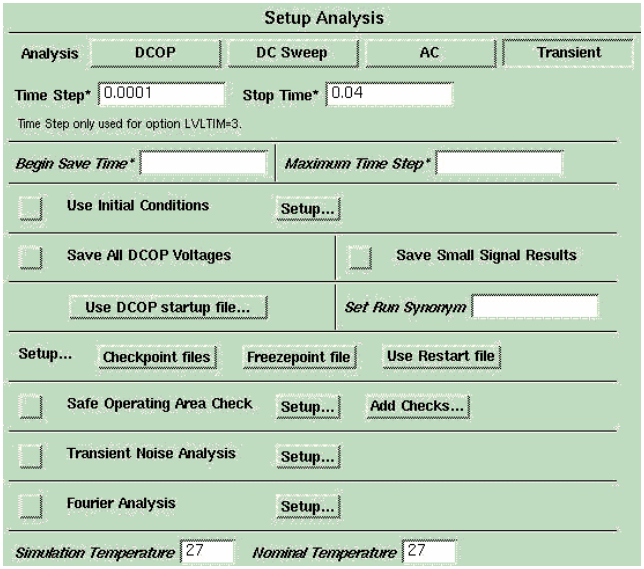
8. Now we are going to add keeps to define the data of the signals which will be saved by Accusim in simulation. Please click palette “Add Keeps”. In the popup window, please click “All”, and click OK to close the window.



9. Now we are going to setup the analysis type. Please click right palette “Setup Analysis”. You will see the popup window as below. Please click “Transient”, and input the following settings:

Time Step: 0.0001
Stop Time: 0.04

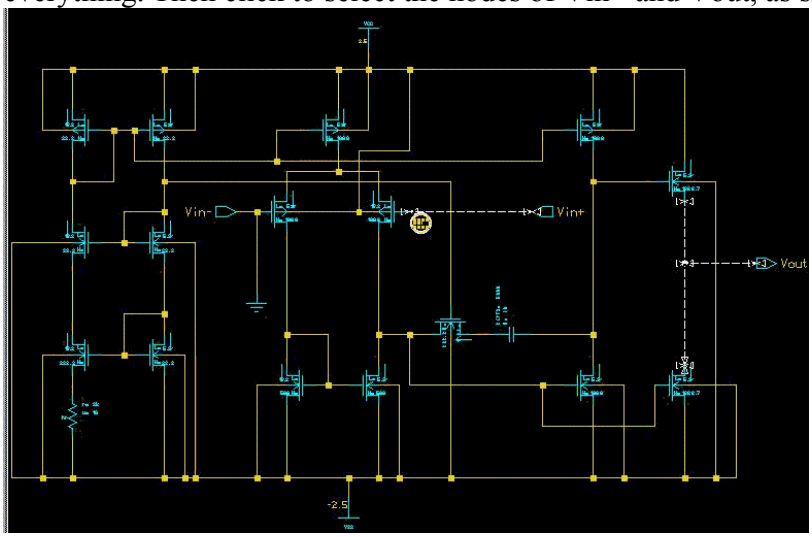
This sets the time step for simulation as 0.0001sec, and total simulation time (stop time) as 0.04sec. We make this setting according to the period of the input signal. Because we already set the frequency of the input Sine voltage in Vin+ port as 100Hz, its period is 0.01sec. By setting the “Stop Time” as 0.04sec, we will get 4 periods of waveforms. For each period of 0.01sec, because the time step is 0.0001sec, we will have 100 data points in each period.



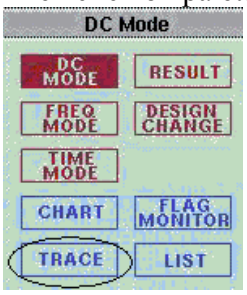
Now please click OK to close the window.

10. Now we are ready to simulate the transient analysis of the circuit. Please click "Run" on the right palette. You will see the simulation is running. When the simulation is complete, you can also view the output file to see whether there is any error. If there is error, use the error information from the output file to help debug it.

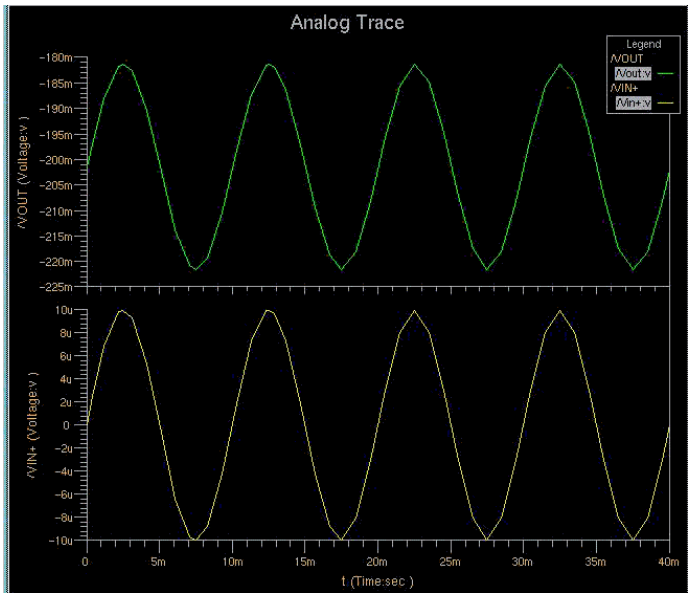
11. We will then trace the signals we are interested in. First press "F2" key in keyboard to unselect everything. Then click to select the nodes of Vin+ and Vout, as shown below.



Then click on palette "Trace",

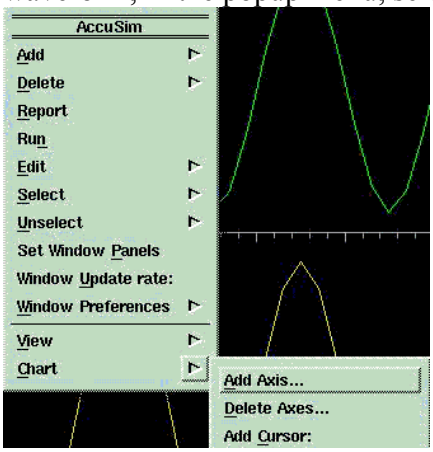


You will see the waveforms for Vin+ and Vout are shown as below.

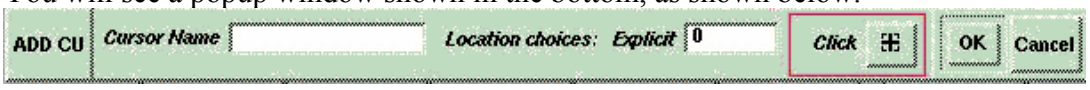


Sometimes the waveforms are hidden behind your schematic, thus you may need to minimize the schematic window to see the waveforms. If you want to add waveforms of other signals, just repeat the above procedure, you would be able to see more signal waveforms.

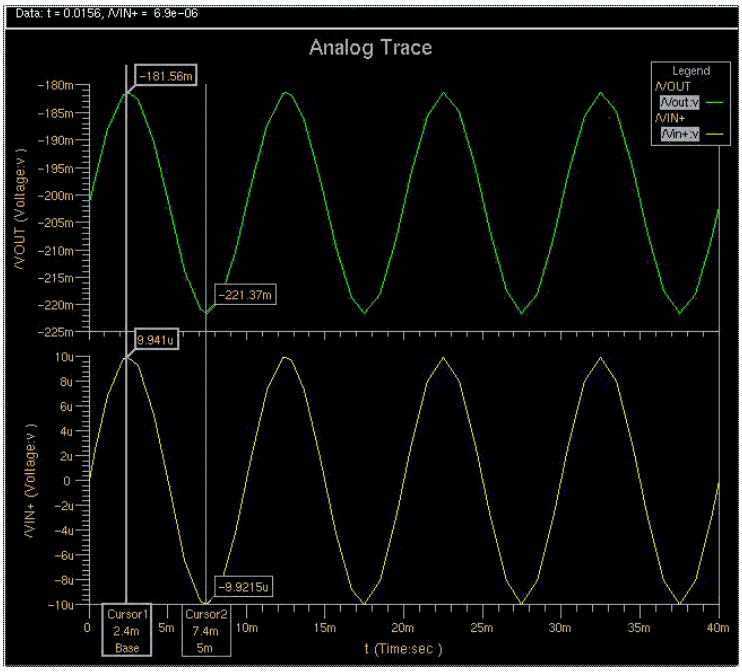
12. In order to measure the gain of the OPAMP, we need to measure the amplitude of the input and output voltages. The cursor can be very helpful in the measurement. Please right click your mouse on the waveform, in the popup menu, select "Chart—Add Cursor", as shown below.



You will see a popup window shown in the bottom, as shown below.



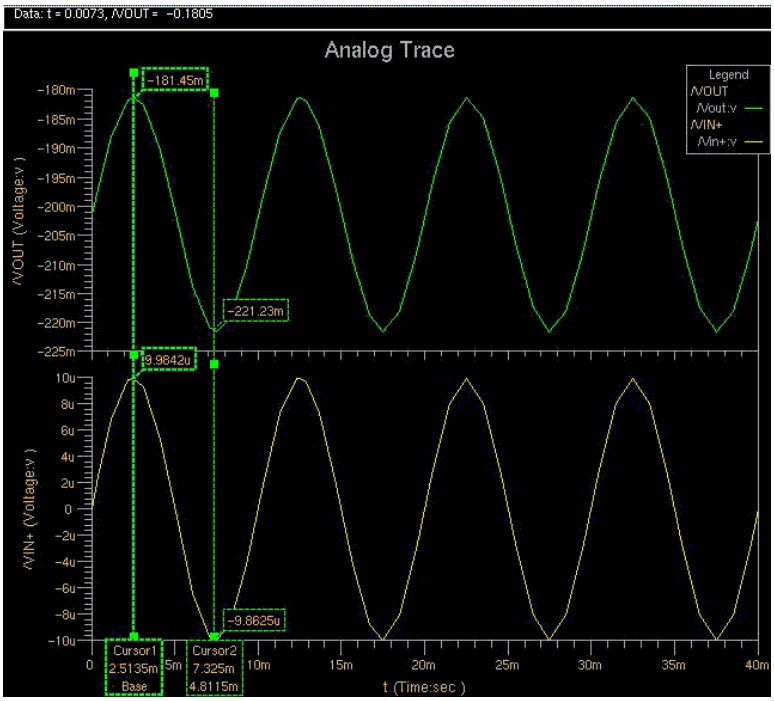
Please click on "Click", and move your mouse on the waveform. You will see a cursor is added to the waveform, and the coordinates of the crosspoint between the cursor and the waveform is continuously displayed in the rectangles. After you put your cursor on the location you are interested in, left click your mouse on that location and the cursor will be fixed at that point. Again, repeat the above procedure to place another cursor on the minimum point of the curves. You needn't worry whether the cursor is located at exactly the minimum point, because you can easily adjust it later. Now your waveform window should look like below.



13. We want to measure the peak-to-peak values of the V(Vin+) and V(Vout). However, your cursor may not be placed exactly on the peak values. It doesn't matter. You can move the cursors easily. Please click on the vertical line of the left cursor, you will see that three small green rectangles appearing in both ends and the middle of the cursor line. Move your mouse to point to exactly the small green rectangle, you will see your mouse change the shape. Now please click on it and drag the cursor line to left or right. The cross point between the cursor line and the waveforms will be dynamically displayed in dotted rectangles. You can observe the change of the crosspoints values to move the cursor to the maximum value of both waveforms, and release the mouse to put the cursor line there. Similarly, you can also move the right cursor line to the minimum points of the curves. Now your curve should look like below. From this measurement, we can easily calculate the gain of the OPAMP:

$$A_v = \frac{(V_{out\_\max} - V_{out\_\min})}{(V_{in\_\max} - V_{in\_\min)}} = \frac{[(-181.45mV) - (-221.23mV)]}{[9.98\mu V - (-9.86\mu V)]}$$

$$= 2005.04V/V = 20\lg(2005.04)dB = 66.04dB$$



14. If the output node is open without load resistor, the voltage gain A_v is:

$$A_v = G_m R_0$$

Where G_m is the transconductance of the OPAMP, and R_0 is the output resistance of the OPAMP.

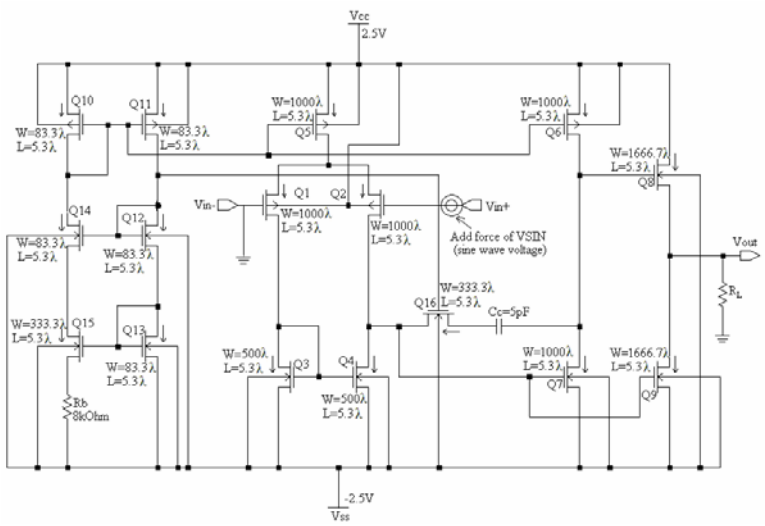
If we connect a known load resistor R_L to the output node, the voltage gain A_v' will become:

$$A_v' = G_m (R_0 \parallel R_L)$$

Thus we have the equation:

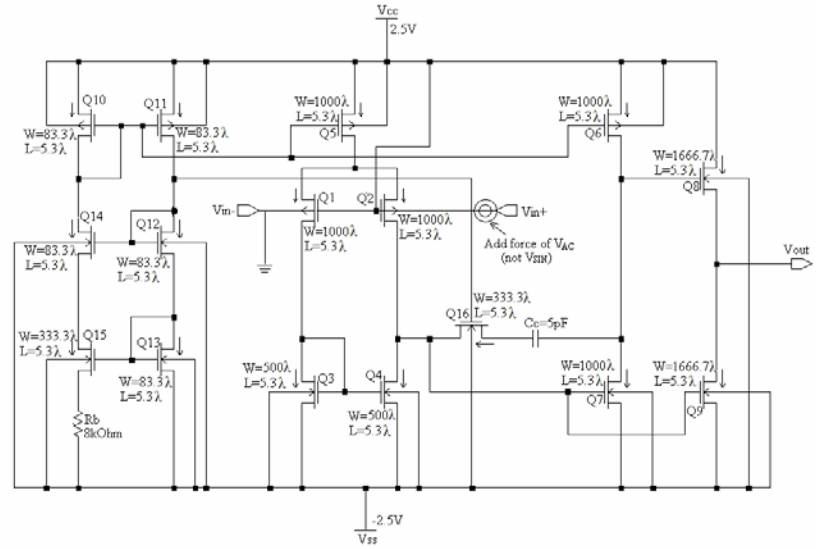
$$\frac{A_v'}{A_v} = \frac{(R_0 \parallel R_L)}{R_0}$$

Using the above procedures to measure the voltage gain with and without load resistance R_L. Put A_v', A_v, and R_L values into the above equation, you can solve it for the output resistance value R_0. Please note that the gain A_v and A_v' should be in unit of V/V instead of dB. If you use dB as the unit for gains, you will get the wrong result for R_0. The circuit structure for transient analysis with load resistor R_L is shown below. As shown in the figure, a load resistor R_L is connected between output port V_{out} and Ground (not Vss). Please note that if you get a distorted output waveform after you add load resistor R_L to V_{out}, you can reduce the amplitude of V_{SIN} applied to Vin+ (for example, set the magnitude as 6μV instead of 200μV). By reducing the input voltage amplitude, you may be able to get undistorted output waveform and find out the gain A_v'.



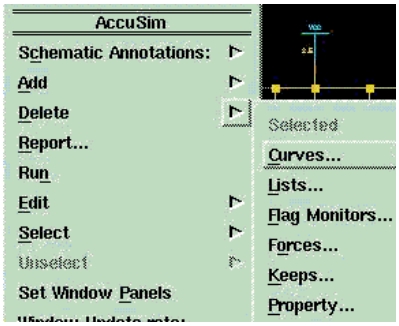
Part 3. AC Frequency Analysis

Up to now we have finished transient analysis. Now let's move on to AC analysis. The circuit structure for AC analysis is shown below.

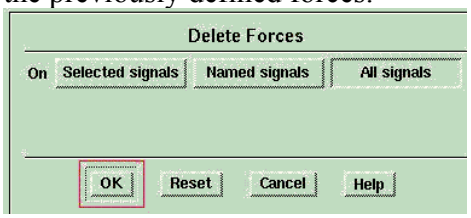


1.For AC analysis, we only need to replace the force of sine wave input in Vin+ with a AC voltage source. Force definition can be performed in Accusim directly, so we needn't go back to the Design Architect. Since model file is already loaded in previous transient analysis, we needn't input it again. Thus we will skip the step for loading library.

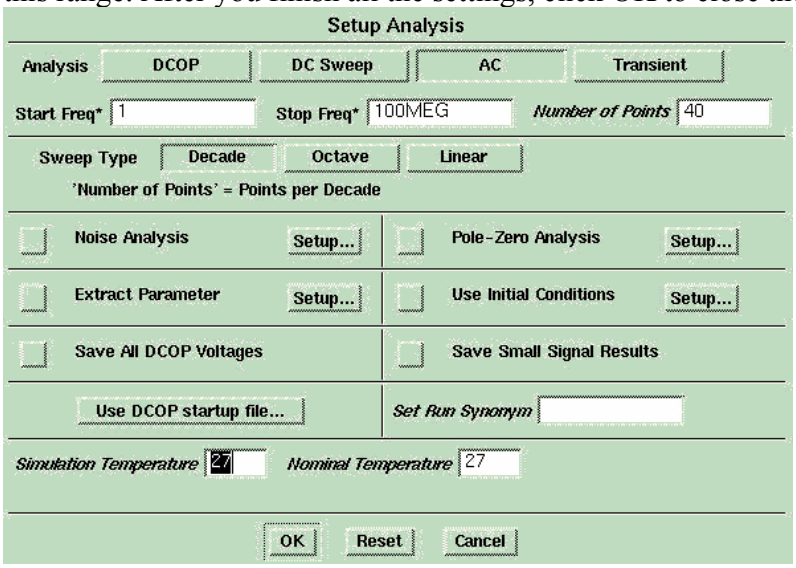
2.Remove all the forced previously defined for transient simulation. Please right click mouse on the design sheet and click to select menu "Delete—Forces".



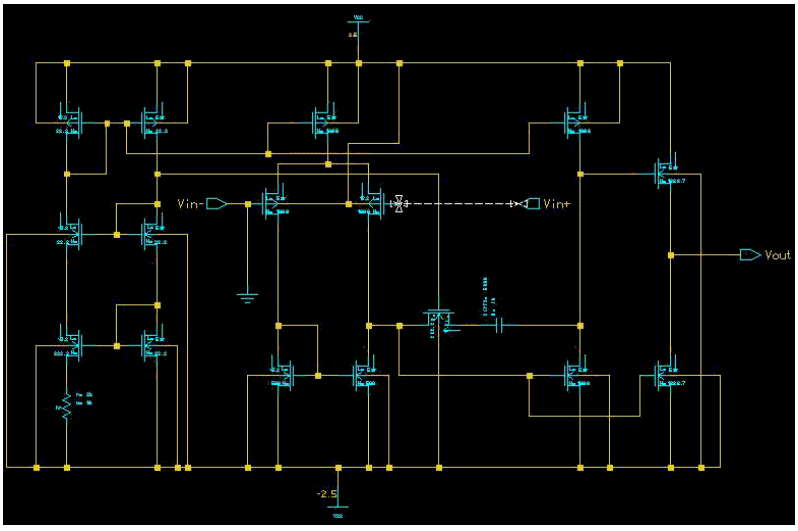
In the popup window, click to select “All signals”, then click OK to close the window. This will delete all the previously defined forces.



3. Now we need to setup the analysis. Please click on palette “Setup Analysis”, you will see following popup window. Please click to select “AC” for “Analysis” row, and input following:
Start Freq*: 1,
Stop Freq*: 100MEG,
Number of Points: 40.
This will set the start frequency as 1Hz, and stop frequency as 100MHz, and 40 points will be simulated in this range. After you finish all the settings, click OK to close the window.



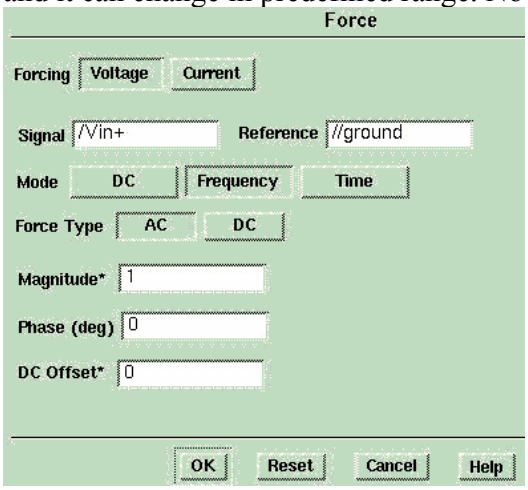
4. Now we are going to define the AC input on Vin+ input port as force. please click to select the Vin+ input port.



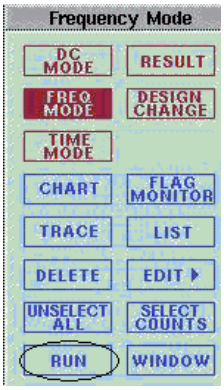
Click palette “Add Force”. You will see following popup window. You can see that the signal is already defined as Vin+, which is the signal you just selected. The reference is “//ground”, this is exactly what we want. Please input the settings as below:

Force type: AC
Magnitude: 1
Phase: 0
DC Offset: 0

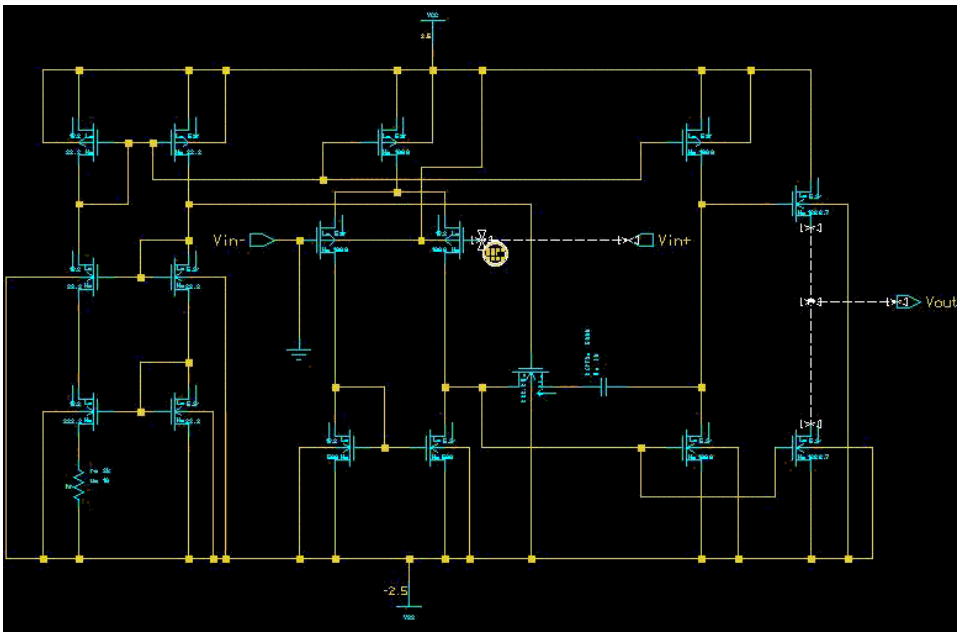
This will apply an AC voltage with magnitude of 1V. In this way, the value of the output voltage can directly stand for the gain (because $A_v=V_{out}/V_{in}=V_{out}/1V=V_{out}$). The frequency of AC voltage is not fixed and it can change in predefined range. Now please click OK to close the window.



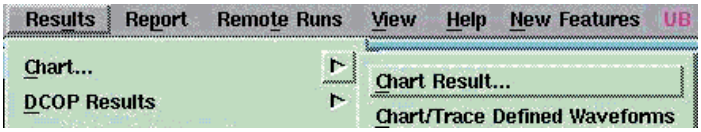
5. Now we are ready for the simulation. Please click on the palette “Run”.



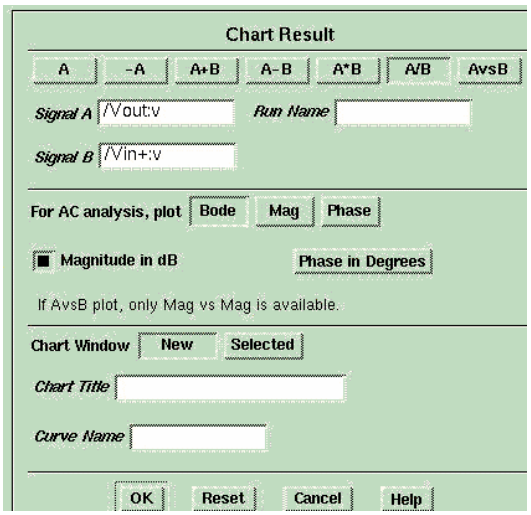
6. You will see your simulation is running. If there is error, try to view the output file to debug the error. If there is no error, you can go ahead to observe the waveforms. First press “F2” to unselect all. Now click to select node connected to port Vout, and then select node connected to port Vin+. Please note that the sequence for selecting the signals does matter. This will define V(Vout) as signal A, and V(Vin+) as signal B, so that we can plot the curve for (A/B) in our next step.



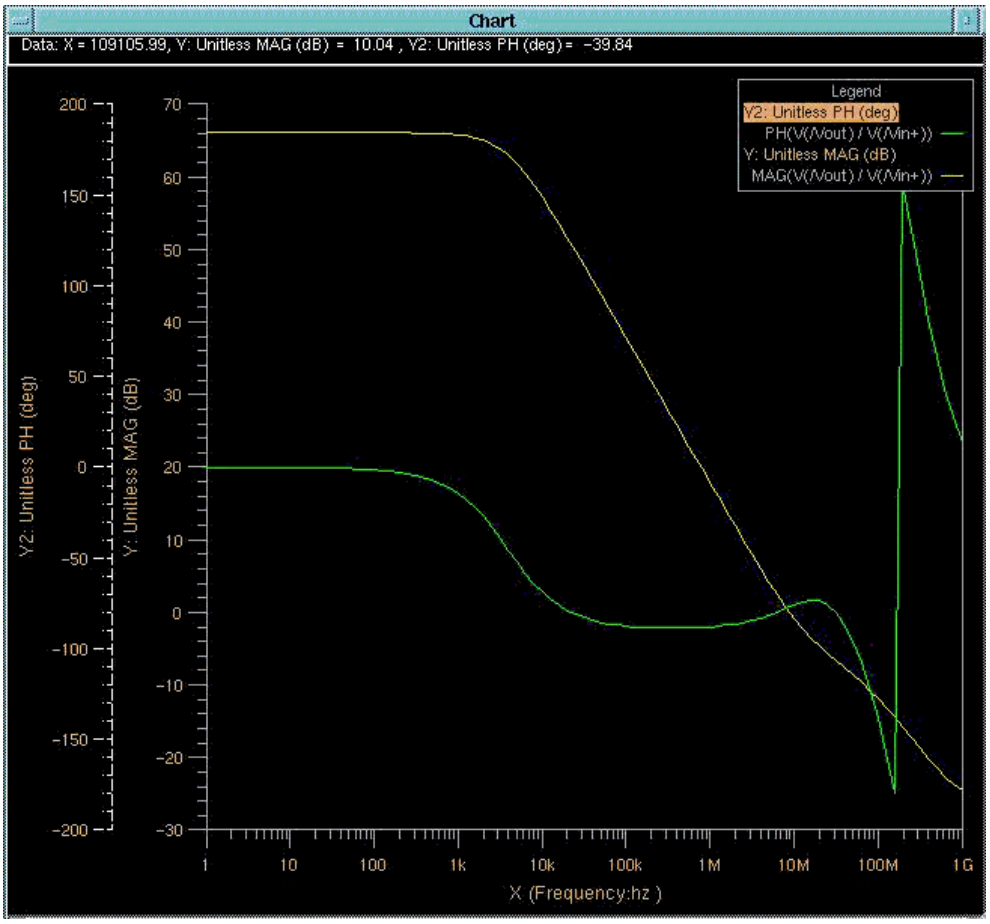
7. Please click to select menu “Results—Chart—Chart Result”.



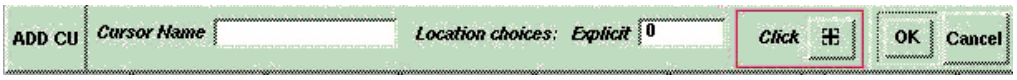
In the popup window, please click “A/B”. You will see signal A is already defined as the fist selected signal (Vout:v), and signal B is defined as the second selected signal (Vin+: v). Please click on “Bode” in “For AC analysis” line. Click OK to close the window.



8. Now you would be able to see the Bode plots for the magnitude and phase angle, as shown below. Sometimes the Bode plot is hidden behind your schematic design. If this is the case, please minimize your Schematic design to see the Bode plot. You can see that the magnitude and phase are plot in the same figure. The X axis is frequency from 1Hz to 100MHz, there are two Y axes: Y1 axis for magnitude in unit of dB, and Y2 axis for phase in unit of degree. The yellow curve is for magnitude, and the green line is for phase.



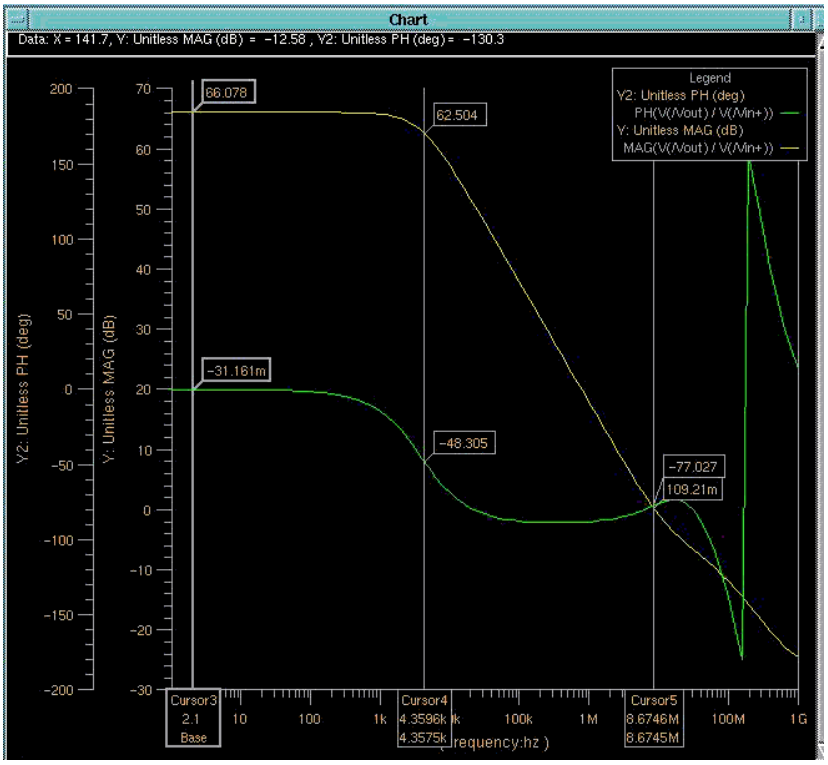
9. From this Bode plot, we can extract valuable information about the circuit, such as midband gain, -3dB frequency, bandwidth BW, unity gain frequency, and phase/gain margin. For example, the flat portion of the Magnitude of the gain indicates midband gain. First please right click your mouse in the waveform window, in the popup menu, select "Chart—Add Cursor". A popup window will be shown in the bottom, as shown below.



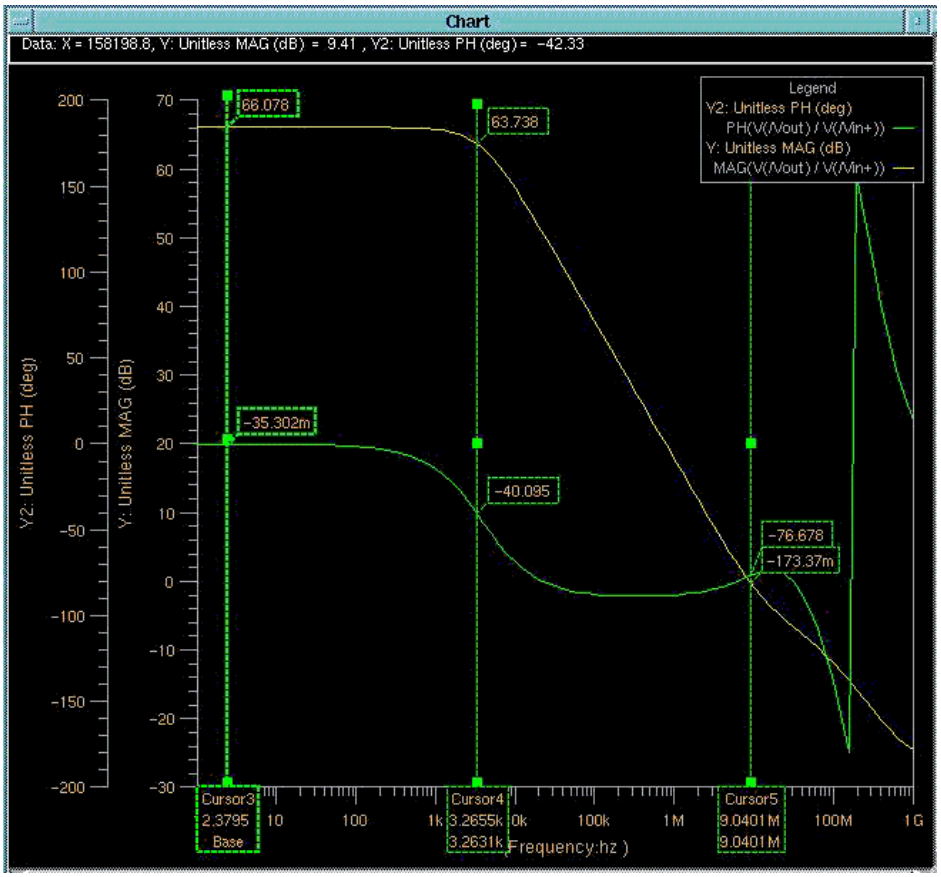
Please click on "Click", and move your mouse on the waveform, and place it anywhere in the flat portion of the magnitude plot. From the cursor, you can read that the midband gain is about 66.1dB. With this information, you can know that the -3dB frequency should correspond to a gain of:
Midband gain-3dB=66.1dB-3dB=63.1dB.

Use the similar procedure to insert a second cursor and place it around -3dB frequency (which corresponds to a gain of about 63.1dB). You may not be able to precisely locate the position at this time. But please don't worry, just insert it in approximate location, and we can adjust it later.

Similarly, insert the third cursor which corresponds to the 0dB gain (unity gain), the corresponding frequency is unity gain frequency (please note 20lg(1V/V)=0dB). You also only need to insert it to the approximate location, and we can further adjust it later. Now your plot may look like below.



10. Now we try to move the cursor to precisely locate them to the desired locations. Please click on -3dB cursor line, and you will see three small rectangles. Place your cursor on one of these cursors, click your mouse and drag it. You will see the crosspoint values are also updated dynamically in the dotted rectangles. Drag it to the location where the magnitude of gain is about 63.1dB, and release the button to place it there. Similarly, move the unity-gain cursor line to the location where the magnitude of gain is about 0dB. Now your plot may look like below.



With Bode plot, we can also find the gain margin and phase margin of the OPAMP. The gain margin is the difference between the open-loop gain and 0dB (unity gain) when phase of the OPAMP is ±180°. The phase margin is the difference between the phase of OPAMP at unity gain frequency and -180°.

11.From the above plot, you can read the following information:
Midband gain: A_M=66.078dB.
-3dB frequency: f_{-3dB}=3.26kHz.
-3dB bandwidth BW=3.26kHz.
Unity gain frequency (or GBP): f_t=9.04MHz.
Unity-gain bandwidth: 9.04MHz.
Phase Margin: PM= -76.678°–(-180°)=103.3°

Congratulations, you have successfully finished Mentor Graphics OPAMP simulation tutorial.